ABSTRACT OF THE DISCLOSURE

A method of generating a truncated scan test pattern for an integrated circuit design includes steps of: (a) receiving as input an integrated circuit design; (b) estimating a number of transition delay fault test patterns and a corresponding number of top-off stuck-at fault patterns to achieve maximum stuck-at fault and transition delay fault coverage; (c) truncating the estimated number of transition delay fault patterns to generate a truncated set of transition delay fault patterns so that the truncated set of transition delay fault patterns and the corresponding number of top-off stuck-at fault patterns achieve maximum stuck-at fault and transition delay fault coverage within a selected scan memory limit; and (d) generating as output the truncated set of transition delay fault patterns and the corresponding number of top-off stuck-at fault patterns.